TA 9.5: An Integrated CMOS Potentiostat for Miniaturized Electroanalytical Instrumentation

Richard J. Reay, Samuel P. Kounaves*, Gregory T. A. Kovacs

Center for Integrated Systems, Stanford University, Stanford, CA
*Department of Chemistry, Tufts University, Medford, MA

Two major limiting factors in mass production and field use of electroanalytical instruments have been the size and cost of potentiostats [1, 2]. This monolithic CMOS potentiostat has performance comparable to bench-top instruments at a fraction of the size, power consumption and cost. Figure 1 shows the block diagram of the potentiostat chip. An integrating DAC sets the voltage between the working electrode, where the electrochemical reactions of interest take place, and a chemically stable reference electrode. The control amplifier regulates this voltage using feedback to drive a third (counter) electrode. The working electrode current is measured with a current-input dual-slope ADC.

Precision switched-capacitor techniques are used throughout to cancel voltage offsets and minimize charge-injection errors. Representative of these techniques is the control amplifier, whose simplified schematic is shown in Figure 2. The desired cell voltage is sampled on C_1 while the amplifier offset and error due to the input switch charge-injection is stored on C_3. The errors are sampled at a second, desensitized amplifier input to minimize further charge-injection errors [3]. A non-return-to-zero technique is used at the desensitized input so the amplifier does not slew to ground during the offset storage phase. Leakage currents are limited to femptoamperes by using only pMOS transistors in n-wells biased at signal ground for all switches connected to the amplifier inputs. Since the amplifier inputs operate as virtual grounds, there is essentially no bias across any parasitic junction at the critical storage nodes, nearly eliminating leakage currents. This leads to a measured output drift of less than 2μV/s using only 5pF storage capacitors, allowing infrequent autozero cycles. The non-inverting amplifier input is connected to the working electrode instead of directly to ground to cancel voltage errors due to the working electrode not being precisely at ground.

The ADC uses similar circuitry to reduce its offset and errors. It is a standard dual-slope integration type converter with an on-chip 10pF integrating capacitor. During the first integration cycle, the working electrode is connected to the integrating node. By changing the length of this cycle, the ADC input can be accurately scaled over an eight-decade range without requiring external matched components.

The schematic of the amplifier used in all three circuit blocks is shown in Figure 3. The amplifier must drive moderate capacitive and large resistive loads with low noise and low systematic offset voltage. It is important to minimize the amplifier offset voltage even though the circuits are offset-compensated, because the amplifier offset is stored at the desensitized inputs of the amplifier. Since the gain of the desensitized input is about eight times lower than that of the main input, the offset plus charge injection is multiplied by eight when it is stored. This amplified offset may cause the parasitic source/n-well junction of the sampling switch to become slightly forward biased, increasing the leakage current. A two-stage topology obtains reasonable gain while driving the resistive load of the electrochemical cell, and cascoded compensation increases the capacitive load capability. Transistors M_1 and M_3 have long channels for good noise performance, and transistor M_4 has a short channel for high capacitive drive capability. This mismatch in channel lengths would normally create a large systematic offset voltage. To avoid this, M_2 is biased in the linear region and acts as a level translator between the two amplifier stages. A replica bias circuit ensures that M_2 has the proper bias over temperature and processing variations.

The prototype chip is fabricated through MOSIS in a 2μm CMOS process (Figure 4). For testing flexibility, reference currents and non-critical digital circuits use off-chip components. The DAC and control amplifier have measured 13b resolution and linearity over a ±4.8V range. The ADC has a minimum resolvable current of 100 fA and a maximum full-scale current of 40μA. For a given input current range, measured resolution and linearity are 13b. For most current ranges, the ADC conversion time is about 3ms for maximum resolution. If only 8b precision is required, the conversion time is 400μs. The chip is connected to a circular thin-film iridium microelectrode in deionized water [4]. A triangular voltage waveform is applied to the microelectrode relative to a solid Ag/AgCl reference electrode. The current is measured to generate an I vs. V plot, 0.5ppm of copper sulfate is added to the solution and a second test is run. Both are shown in Figure 5. The increase in current at the potential extremes of the plot is due to electrolysis of the water and oxygen reactions. The peak at about 100mV is due to copper oxidation.

The potentiostat chip works well for this and other electrochemical experiments performed. The next version includes on-chip current references to allow single-supply operation. When combined with an inexpensive microcontroller, a battery, and a microelectrode chip, a complete computer-controlled electrochemical analysis system is formed that requires only a few cubic cm. The performance of this system is comparable to quality bench-top potentiostats, as summarized in Table 1 [5]. This device lowers the cost, size, and weight of electroanalytical instrumentation and opens up applications in many areas.

Acknowledgments

This work is funded by grants from EPA, Stanford CIS, Northeast Hazardous Substance Research Center, EG&G PARC, NSF (CHE-9256871), and the Robert N. Noyce Family Faculty Scholar Chair (Kovacs). R. Reay is supported by a NSF Graduate Fellowship.

References

[1] Bard, A., L. Faulkner, *Electrochemical Methods*, New York: John Wiley & Sons, 1980, pp. 563-567.

[2] Turner, R., et al., "A CMOS Potentiostat for Amperometric Chemical Sensors," IEEE Jour. Solid-State Circuits , v.22, n.3, pp. 473-478, June 1987.

[3] Degrauwe, M., et al, "A Micropower CMOS-Instrumentation Amplifier," IEEE Jour. Solid-State Circuits , v. 20, n. 3, pp. 805-807, June 1985.

[4] Kovacs, G., et al, "Regeneration Microelectrode Array for Peripheral Nerve Recording and Stimulation," IEEE Trans. on Bio. Eng., v. 39, n. 8, pp. 893-902, Sept. 1992.

[5] Model 273A Potentiostat/Galvanostat data sheet, EG&G Princeton Applied Research, Princeton, NJ.

0-7803-1844-7 / 94 / $3.00 / © 1994 IEEE

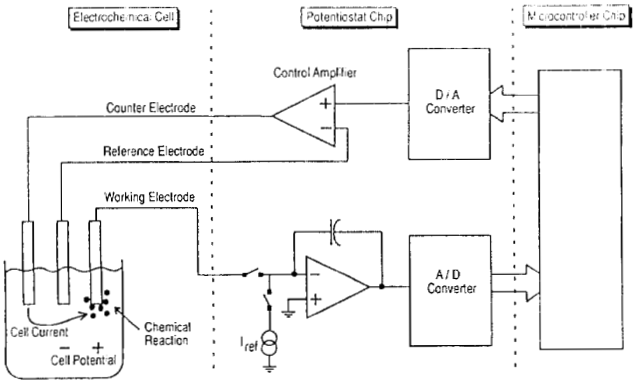

Figure 1: Block diagram of potentiostat system.

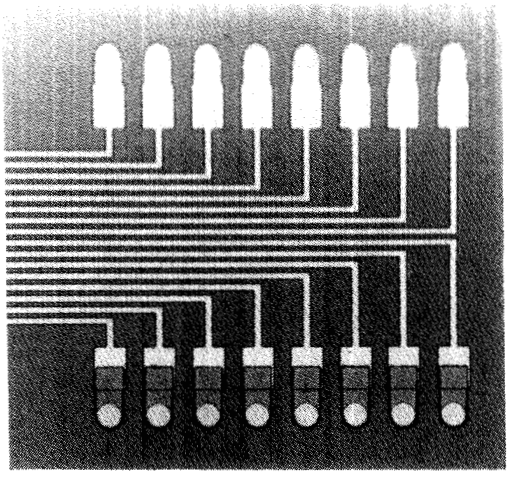

Figure 4: Micrograph of microelectrode array, gold (bottom), iridium (top) electrodes.

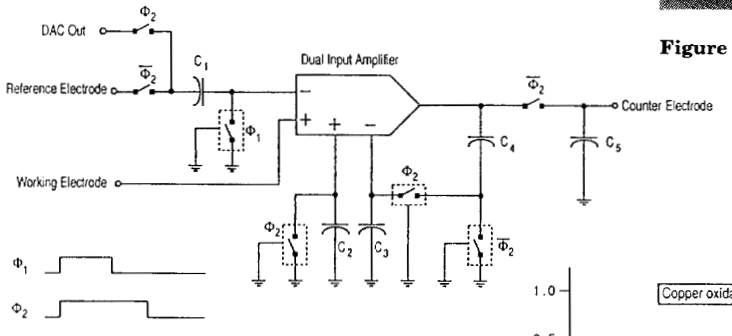

Figure 2: Control amplifier schematic.

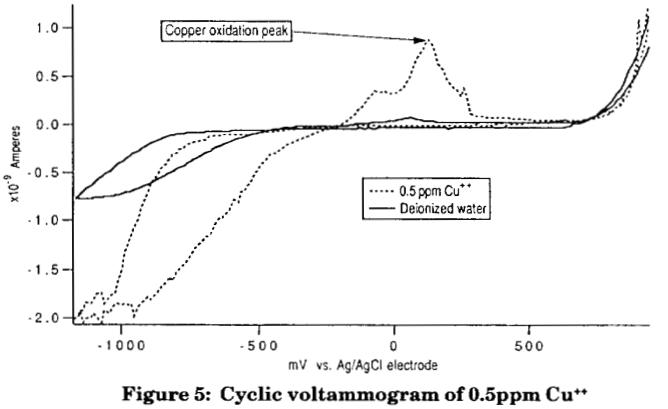

Figure 5: Cyclic voltammogram of 0.5ppm Cu^{++} solution measured with potentiostat system.

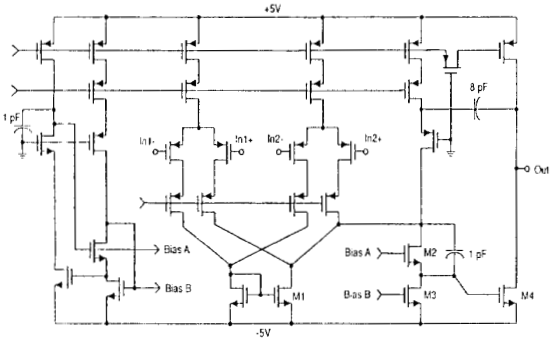

Figure 3: Amplifier schematic.

Parameter	Potentiostat	EG&G 237A
DAC range	±4.8V	±8V
DAC resolution	13b	14b
ADC dynamic range	100fA to 40mA	2pA to 1A
ADC accuracy	0.02% of range	0.5% of range
Max sample rate	2.5kHz	20kHz
Power	5mW	350W
Size	2.2x2.2mm^2	48x30x51cm
Weight	<<1g	31kg

Table 1: Performance comparison of potentiostat chip and EG&G PAR Model 273A potentiostat.